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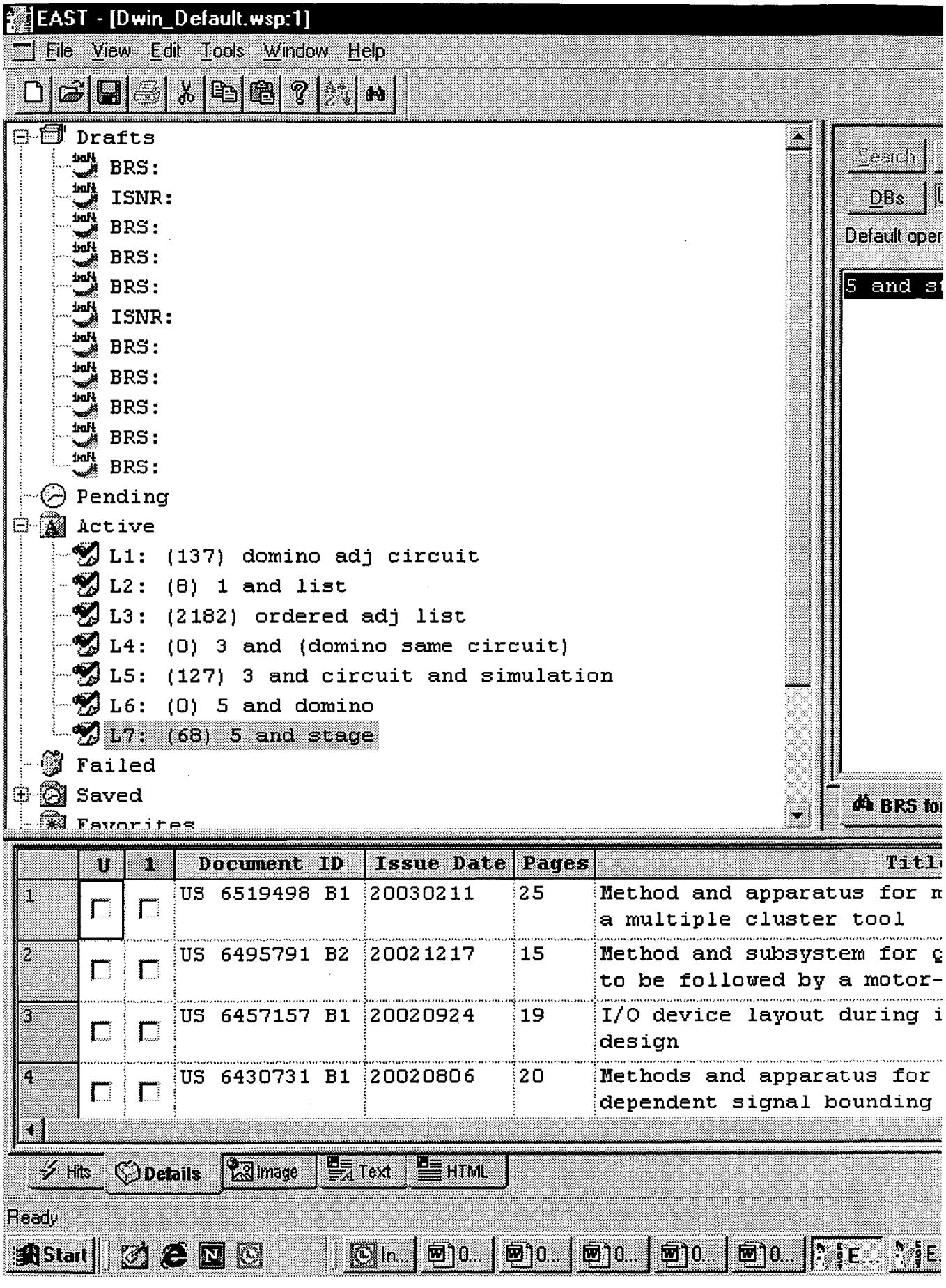
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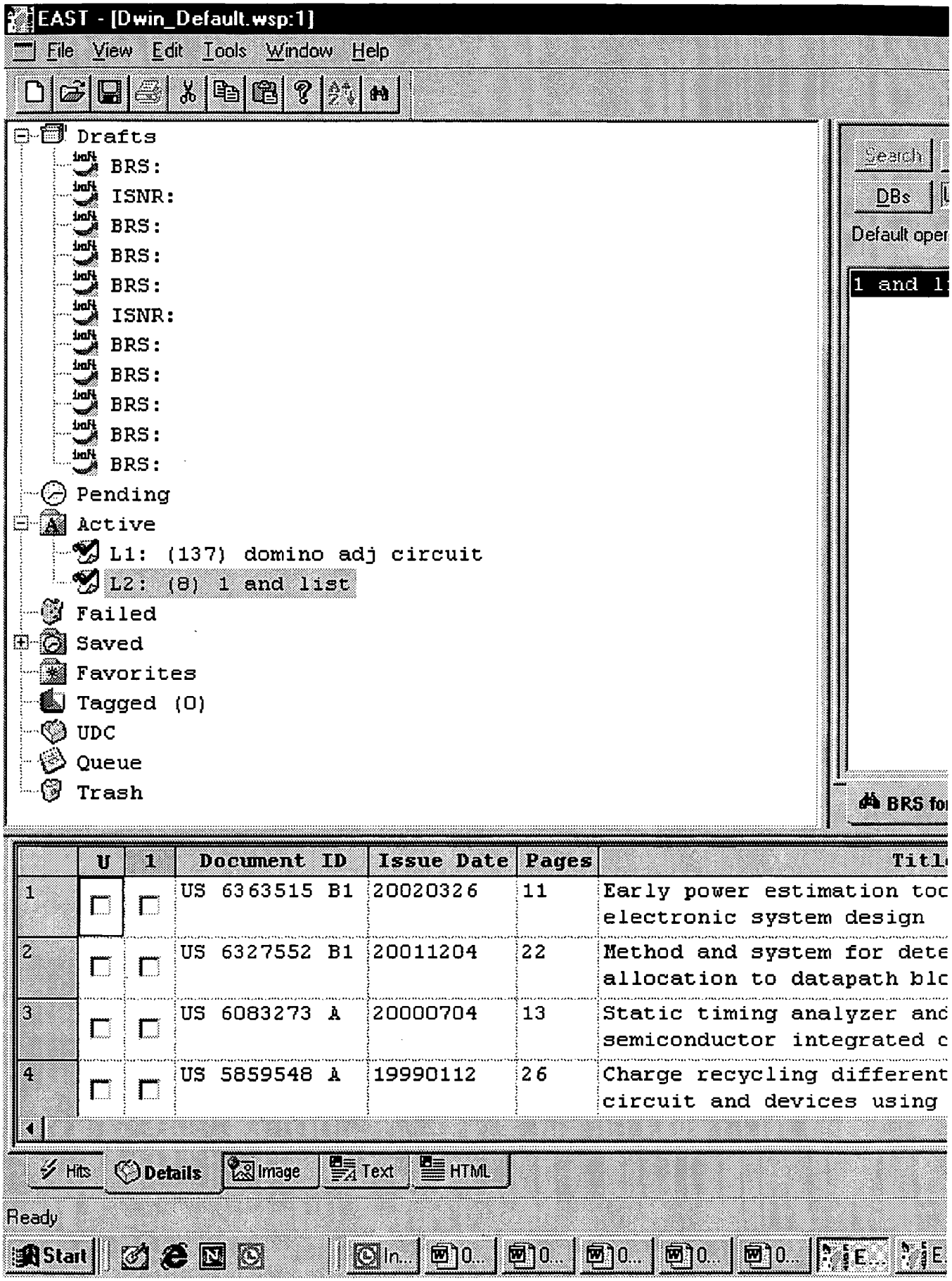
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Arani Sinha , Sandeep K. Gupta , Melvin A. Breuer
Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design
November 1999
Inductance of on-chip interconnects gives rise to signal overshoots and undershoots that can cause logic errors. By considering technology trends, we show that in 0.13 &mgr;m technology such noise in local interconnects embedded in combinational logic can exceed the threshold voltage. We show the impact of such noise on different kinds of circuits. The magnitude of this noise can increase due to process variations. We present an algorithm for generating vectors for ...

2 Noise-aware power optimization for on-chip interconnect 85%
Ki-Wook Kim , Seong-Ook Jung , Unni Narayanan , C. L. Liu , Sung-Mo Kang
Proceedings of the 2000 international symposium on Low power electronics and design
August 2000
Realization of high-performance domino logic depends strongly on energy-efficient and noise-tolerant interconnect design in ultra deep sub-micron processes. We characterize the cycle-averaged power model for interconnects accounting for switching statistics and dynamic behaviors. For the sake of signal integrity, cross-coupling effects are also characterized which reflect logical correlation between adjacent wires. Based on the new models for interconnect power and capacitive crosstalk, we ...

3 Future Design Trends: A roadmap and vision for physical design 80%

Andrew B. Kahng
Proceedings of the 2002 international symposium on Physical design April 2002
This invited paper offers "roadmap and vision" for physical design. The main messages are as follows. (1) The high-level roadmap for physical design is static and well-known. (2) Basic problems remain untouched by fundamental research. (3) Academia should not overemphasize back- filling and formulation over innovation and optimization. (4) The physical design field must become more mature and efficient in how it prioritizes research directions and uses its human resources. (5) The scope of physi ...

4 Design issues for dynamic voltage scaling 80%
Thomas D. Burd , Robert W. Brodersen
Proceedings of the 2000 international symposium on Low power electronics and design August 2000
Processors in portable electronic devices generally have a computational load which has time-varying performance requirements. Dynamic Voltage Scaling is a method to vary the processors supply voltage so that it consumes the minimal amount of energy by operating at the minimum performance level required by the active software processes. A dynamically varying supply voltage has implications on the processor circuit design and design flow, but with some minimal constraints it is straightforwa ...

5 Energy and Delay Considerations: Low swing dual threshold voltage domino logic 80%
Volkan Kursun , Eby G. Friedman
Proceedings of the 12th ACM Great Lakes Symposium on VLSI April 2002
A low swing domino logic technique is proposed to decrease power consumption without sacrificing noise immunity. With the proposed low swing domino logic circuit technique, active power consumption is reduced by up to 9.4% while improving the noise immunity by 2.6% as compared to standard domino logic circuits. It is also shown that by applying a low swing contention reduction technique, the power savings can be further increased by 6.7% while the delay can be improved by 8.6%. A simple and effi ...

6 Wang Tiles for image and texture generation 77%
Michael F. Cohen , Jonathan Shade , Stefan Hiller , Oliver Deussen
ACM Transactions on Graphics (TOG) July 2003
Volume 22 Issue 3
We present a simple stochastic system for non-periodically tiling the plane with a small set of Wang Tiles. The tiles may be filled with texture, patterns, or geometry that when assembled create a continuous representation. The primary advantage of using Wang Tiles is that once the tiles are filled, large expanses of non-periodic texture (or patterns or geometry) can be created as needed very efficiently at runtime.Wang Tiles are squares in which each edge is assigned a color. A valid tiling req ...

7 Rule-based VLSI verification system constrained by layout parasitics 77%
J. Wenin , J. Verhasselt , M. Van Camp , J. Leonard , P. Guebels
Proceedings of the 1989 26th ACM/IEEE conference on Design automation conference June 1989
This paper addresses a rule-based method for VLSI design review, constrained by parasitics. Using the new ideas discussed in this paper, extraction from layout is not limited anymore to

conventional electrical data, but additionally allows modelling of functional and timing behaviour. An extendable rule based validation algorithm operates on extracted models, decorated with parasitic effects, to formally prove most aspects of design correctness.

8 Session 6C: Signal integrity and clock design: CASh: a novel "clock as shield" design methodology for noise immune precharge-evaluate logic 77%

Yonghee Im , Kaushik Roy

Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design November 2001

In gigascale integrated circuits (GSI), interconnects are expected to play a more dominant role in circuit performance than transistor cells. The circuit performance is affected by signal integrity as cross-talk becomes more significant with the scaling of feature sizes. Many attempts have been made to improve noise immunity, but all require the sacrifice of speed as a trade-off, especially in dynamic circuits. Avoiding noise problems while maintaining the desired speed would involve increased w ...

9 Suggestions for a method of analyzing binary images using Langlet's parity logic 77%

Stuart Smith

ACM SIGAPL APL Quote Quad , Proceedings of the 2001 conference on APL: an arrays odyssey December 2000

Volume 31 Issue 2

This paper describes an extension to the system of parity logic operations developed by Gerard Langlet and subsequently elaborated by Michael Zaus. Two operations, A and B, are introduced which can be used both to analyze and to synthesize arbitrary patterns of l's and O's in square Boolean matrices. The A and B operations are, like most of the operations in Langlet's system, completely reversible (i.e., the input to A or B can be exactly rec ...

10 New test methods targeting non-classical faults: A novel wavelet transform based transient current analysis for fault detection and localization 77%

Swarup Bhunia , Kaushik Roy , Jaume Segura

Proceedings of the 39th conference on Design automation June 2002

Transient current (IDD) based testing has been often cited and investigated as an alternative and/or supplement to quiescent current (IDDQ) testing. While the potential of IDD testing for fault detection has been established, there is no known efficient method for fault diagnosis using IDD analysis. In this paper, we present a novel integrated method for fault detection and localization using wavelet transform based IDD waveform analysis. The time-frequency resolution property of wavelet transfo ...

11 Future performance challenges in nanometer design 77%

Dennis Sylvester , Himanshu Kaul

Proceedings of the 38th conference on Design automation June 2001

We highlight several fundamental challenges to designing high-performance integrated circuits in nanometer-scale technologies (i.e. draRita Glover, EDA Today, L.C.wn feature sizes< 100 nm). Dynamic power scaling trends lead to major packaging problems. To alleviate these concerns, tMarc Halpernhermal monitoring and feedback mechanisms can limit worst-case dissipation and reduce costs. Furthermore, a flexible multi-Vdd + multi-Vth + re-sizing approach is advocated to leverage the inherent pr ...

12 False coupling interactions in static timing analysis 77%

Ravishankar Arunachalam , Ronald D. Blanton , Lawrence T. Pileggi

Proceedings of the 38th conference on Design automation June 2001

Neighboring line switching can contribute to a large portion of the delay of a line for today's deep submicron designs. In order to avoid excessive conservatism in static timing analysis, it is important to determine if aggressor lines can potentially switch simultaneously with the victim. In this paper, we present a comprehensive ATPG-based approach that uses functional information to identify valid interactions between coupled lines. Our algorithm accounts for glitches on aggressors that ...

13 Is nanometer design under control? (panel session) 77%

Andrew B. Kahng , Nancy Nettleton , John Cohn , Shekhar Borkar , Louis Scheffer , Ed Cheng , Sang Wang

Proceedings of the 38th conference on Design automation June 2001

As fabrication technology moves to 100 nm and below, profound nanometer effects become critical in developing silicon chips with hundreds of millions of transistors. Both EDA suppliers and system houses have been re- tooling, and new methodologies have been emerging. Will these efforts meet the challenges of nanometer silicon such as performance closure, power, reliability, manufacturability, and cost? Which aspects of nanometer design are, or are not, under control? This session will consi ...

14 Transistor sizing for reliable domino logic design in dual threshold voltage technologies 77%

Seong-Ook Jung , Ki-Wook Kim , Sung-Mo Steve Kang

Proceedings of the 11th Great Lakes Symposium on VLSI March 2001

15 Reliability Issues in Computing System Design 77%

B. Randell , P. Lee , P. C. Treleaven

ACM Computing Surveys (CSUR) June 1978

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16 Studies in machine cognition using the game of poker 77%

Nicholas V. Findler

Communications of the ACM April 1977

Volume 20 Issue 4

A progress report is presented of on-going research efforts concerning human decision making under uncertainty and risk and human problem solving and learning processes on the one hand, and machine learning, large scale programming systems, and novel programming techniques on the other. There has also been interest in how humans make deductive and inductive inferences and form and optimize heuristic rules, and how machines can reach similar results. Although the vehicle of these investigati ...

17 Curriculum 68: Recommendations for academic programs in computer science: a report of the ACM curriculum committee on computer science 77%

William F. Atchison , Samuel D. Conte , John W. Hamblen , Thomas E. Hull , Thomas A. Keenan , William B. Kehl , Edward J. McCluskey , Silvio O. Navarro , Werner C. Rheinboldt ,

Earl J. Schweppe , William Viavant , David M. Young
Communications of the ACM March 1968
Volume 11 Issue 3

18 Teaching C++ in a multi-user virtual environment 77%
J. Mark Pullen , Eugene Norris , Mark Fix
ACM SIGCSE Bulletin June 2000
Volume 32 Issue 2
The Internet has opened tremendous possibilities for distance education, where teachers and students can be distributed worldwide. However, much of today's Internet-based teaching is limited to student access of Web-based multimedia documents. In this paper we describe new dimensions in distributed education that are possible in synchronous sessions where the students interact with the teacher in real time. We review and elaborate on the nature of the MUVE, a spatially oriented, network-accessed ...

19 ClariNet: a noise analysis tool for deep submicron design 77%
Rafi Levy , David Blaauw , Gabi Braca , Aurobindo Dasgupta , Amir Grinshpon , Chanlee Oh , Boaz Orshav , Supamas Sirichotiyakul , Vladimir Zolotov
Proceedings of the 37th conference on Design automation June 2000
Coupled noise analysis has become a critical issue for deep-submicron, high performance design. In this paper, we present, ClariNet, an industrial noise analysis tool, which was developed to efficiently analyze large, high performance processor designs. We present the overall approach and tool flow of ClariNet and discuss three critical large-processor design issues which have received limited discussion in the past. First, we present how the driver gates of a coupled interconnect network a ...

20 “Timing closure by design,” a high frequency microprocessor design methodology 77%
S. Posluszny , N. Aoki , D. Boerstler , P. Coulman , S. Dhong , B. Flachs , P. Hofstee , N. Kojima , O. Kwon , K. Lee , D. Meltzer , K. Nowka , J. Park , J. Peter , J. Silberman , O. Takahashi , P. Villarrubia
Proceedings of the 37th conference on Design automation June 2000
This paper presents a design methodology emphasizing early and quick timing closure for high frequency microprocessor designs. This methodology was used to design a Gigahertz class PowerPC microprocessor with 19 million transistors. Characteristics of “Timing Closure by Design are 1) logic partitioned on timing boundaries, 2) predictable control structures (PLAs), 3) static interfaces for dynamic circuits, 4) low skew clock distribution, 5) deterministic method of macro placement, 6) ...

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ASIC/SOC Conference, 2002. 15th Annual IEEE International , 25-28 Sept. 2002
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[Abstract] [PDF Full-Text (336 KB)] **IEEE CNF**

2 **Crosstalk fault reduction and simulation for clock-delayed domino circ**
Shimizu, K.; Itazaki, N.; Kinoshita, K.;
Test Symposium, 2002. (ATS '02). Proceedings of the 11th Asian , 18-20 Nov. 2
Page(s): 176 -181

[Abstract] [PDF Full-Text (1636 KB)] **IEEE CNF**

3 **Dynamic logic styles with improved noise-immunity**
Mendoza-Hernandez, F.; Linarea, M.; Champac, V.H.;
Devices, Circuits and Systems, 2002. Proceedings of the Fourth IEEE Internation Caracas Conference on , 17-19 April 2002
Page(s): C031-1 -C031-5

[Abstract] [PDF Full-Text (508 KB)] **IEEE CNF**

4 **Optimal timing for skew-tolerant high-speed domino logic**
Seong-Ook Jung; Ki-Wook Kim; Sung-Mo Kang;
VLSI, 2003. Proceedings. IEEE Computer Society Annual Symposium on , 25-26 2002
Page(s): 34 -39

[Abstract] [PDF Full-Text (292 KB)] **IEEE CNF**

5 **Noise constrained transistor sizing and power optimization for dual V/ domino logic**
Seong-Ook Jung; Ki-Wook Kim; Sung-Mo Kang;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 10 5 , Oct. 2002
Page(s): 532 -541

[Abstract] [PDF Full-Text (769 KB)] **IEEE JNL**

6 **Robustness of sub-70 nm dynamic circuits: analytical techniques and s trends**
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VLSI Circuits, 2001. Digest of Technical Papers. 2001 Symposium on , 14-16 Jun

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[Abstract] [PDF Full-Text (212 KB)] **IEEE CNF**

7 **Testing of dynamic logic circuits based on charge sharing**
Heragu, K.; Sharma, M.; Kundu, R.; Blanton, R.D.;
VLSI Test Symposium, 19th IEEE Proceedings on. VTS 2001 , 29 April-3 May 20
Page(s): 396 -403

[Abstract] [PDF Full-Text (592 KB)] **IEEE CNF**

8 **Variable threshold voltage keeper for contention reduction in dynamic circuits**
Kursun, V.; Friedman, E.G.;
ASIC/SOC Conference, 2002. 15th Annual IEEE International , 25-28 Sept. 2002
Page(s): 314 -318

[Abstract] [PDF Full-Text (419 KB)] **IEEE CNF**

9 **Fault simulation method for crosstalk faults in clock-delayed domino C circuits**
Shimizu, K.; Takamura, M.; Shirai, T.; Itazaki, N.; Kinoshita, K.;
Electronic Design, Test and Applications, 2002. Proceedings. The First IEEE International Workshop on , 29-31 Jan. 2002
Page(s): 92 -96

[Abstract] [PDF Full-Text (252 KB)] **IEEE CNF**

10 **Test vector generation for charge sharing failures in dynamic logic**
Heragu, K.; Sharma, M.; Kundu, R.; Blanton, R.D.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions o
Volume: 21 Issue: 12 , Dec. 2002
Page(s): 1502 -1508

[Abstract] [PDF Full-Text (363 KB)] **IEEE JNL**

11 **A contention-free domino logic for scaled-down CMOS technologies w ultra low threshold voltages**
Elraba, M.E.S.; Anis, M.H.; Elmasry, M.I.;
Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on , Volume: 1 , 28-31 May 2000
Page(s): 748 -751 vol.1

[Abstract] [PDF Full-Text (252 KB)] **IEEE CNF**

12 **Synthesis of CMOS domino circuits for charge sharing alleviation**
Ching-Hwa Cheng; Shih-Chieh Chang; Shin-De Li; Wen-Ben Jone; Jinn-Shyan W
Computer Aided Design, 2000. ICCAD-2000. IEEE/ACM International Conference
5-9 Nov. 2000
Page(s): 387 -390

[Abstract] [PDF Full-Text (396 KB)] **IEEE CNF**

13 **CASh: a novel "Clock As Shield" design methodology for noise immun precharge-evaluate logic**
Yonghee Im; Roy, K.;
Computer Aided Design, 2001. ICCAD 2001. IEEE/ACM International Conference
4-8 Nov. 2001
Page(s): 337 -341

[Abstract] [PDF Full-Text (411 KB)] **IEEE CNF**

14 **1998 IEEE/ACM International Conference on Computer-Aided Design Digest of Technical Papers (IEEE Cat. No.98CB36287)**
Computer-Aided Design, 1998. ICCAD 98. Digest of Technical Papers. 1998 IEEE International Conference on , 8-12 Nov. 1998

[Abstract] [PDF Full-Text (644 KB)] **IEEE CNF**

15 **GateMaker: a transistor to gate level model extractor for simulation, automatic test pattern generation and verification**
Kundu, S.;
Test Conference, 1998. Proceedings. International , 18-23 Oct. 1998
Page(s): 372 -381

[Abstract] [PDF Full-Text (768 KB)] **IEEE CNF**

---

16 **Noise-tolerant dynamic circuit design**
Lei Wang; Shanbhag, N.R.;
Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE Internatio
Symposium on , Volume: 1 , 30 May-2 June 1999
Page(s): 549 -552 vol.1

[Abstract] [PDF Full-Text (372 KB)] **IEEE CNF**

---

17 **Design of domino CMOS cells under delay constraint**
Zamudio, A.; Champac, V.H.; Sarmiento-Reyes, A.;
Design of Mixed-Mode Integrated Circuits and Applications, 1999. Third Internat
Workshop on , 26-28 July 1999
Page(s): 106 -109

[Abstract] [PDF Full-Text (284 KB)] **IEEE CNF**

---

18 **Energy-efficiency bounds for noise-tolerant dynamic circuits**
Shanbhag, N.R.; Wang, L.;
Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE
International Symposium on , Volume: 4 , 28-31 May 2000
Page(s): 273 -276 vol.4

[Abstract] [PDF Full-Text (304 KB)] **IEEE CNF**

---

19 **Skew-tolerant high-speed (STHS) domino logic**
Seong-Ook Jung; Seung-Moon Yoo; Ki-Wook Kim; Sung-Mo Kang;
Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposiu
Volume: 4 , 6-9 May 2001
Page(s): 154 -157 vol. 4

[Abstract] [PDF Full-Text (320 KB)] **IEEE CNF**

---

20 **Sub-Domino logic: ultra-low power dynamic sub-threshold digital log**
Soeleman, H.; Roy, K.; Paul, B.;
VLSI Design, 2001. Fourteenth International Conference on , 3-7 Jan. 2001
Page(s): 211 -214

[Abstract] [PDF Full-Text (336 KB)] **IEEE CNF**

21 **An energy-efficient noise-tolerant dynamic circuit technique**
Wang, L.; Shanbhag, N.R.;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transaction
Volume: 47 Issue: 11 , Nov 2000
Page(s): 1300 -1306

[Abstract] [PDF Full-Text (212 KB)] **IEEE JNL**

22 **Timing constraints for domino logic gates with timing-dependent kee**
Seong-Ook Jung; Ki-Wook Kim; Sung-Mo Kang;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions o
Volume: 22 Issue: 1 , Jan. 2003
Page(s): 96 -103

[Abstract] [PDF Full-Text (473 KB)] **IEEE JNL**